are not overlapped by the layer 5). Applicant understands that the Examiner does not dispute the description of this and related features with respect to top-gate TFTs.

Further, the specification recites at page 14, lines 9-11 that "the present invention can be applied to a bottom gate type transistor in which a gate electrode is located below the channel forming region." Therefore, Applicant respectfully submits that the descriptions of a construction, structure, and function of the top gate type transistor are equally or similarly applicable in the case of a bottom gate type transistor, so that FIG. 5 merely illustrates that which is already described in Applicant's specification.

In particular, and with respect to FIGS. 1A-1E and associated description, Applicant submits that the specification describes a technique by which a first conductive film and a second conductive film are deposited over an insulating substrate (e.g., by a sputtering technique). A planar insulating layer 3 may then be formed thereover by, for example, plasma CVD methodology. As referenced above, these and related techniques also may be used in the formation of a bottom gate type transistor. Therefore, Applicant respectfully disagrees with the assertion of paragraph 2, section b, of the Office Action that the specification, as originally filed, fails to describe "the semiconductor region being formed over the gate and interposed insulating layer so as to be planar" as illustrated in FIG. 5, and requests that this objection be withdrawn.

Therefore, based on the above, and regarding the rejection of 1, 44-48, and 55-84 under 35 U.S.C. 112, first paragraph, Applicant respectfully submits that all of claims 1, 44-48, and 55-84 are fully described within Applicant's specification.

In particular, the Office Action asserts at paragraph 4, section a, that the specification as filed does not disclose for a bottom gate type transistor, "extending portions of the first conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said first conductive layer." In response, and as should be apparent from the above discussion, Applicant submits that these features are illustrated in, for example, FIGS. 2B and 2C.

The Office Action further asserts in paragraph 4, section b., that, with respect to claims 45-48, the specification as filed does not disclose for a bottom gate type transistor that "a

distance between the first portion and the source were drain region is either larger than, equal to, or less then a thickness of the second conductive layer." In response, Applicant respectfully submits that these features are illustrated in, for example, FIGS. 2B-2D, and with reference to the distances labeled x_o, t_1, and/or t_2 and associated discussion within Applicant's specification.

Based on the above, Applicant respectfully submits that FIG. 5 does not constitute new matter, and that claims 1, 44-48, and 55-84 comply with all of the requirements of 35 U.S.C. 112, first paragraph, and are in condition for allowance. Therefore, Applicant respectfully requests such action in the Examiner's next official communication.

As a final matter, Applicant respectfully submits that the present Office Action has been improperly made final. In particular, Applicant submits that Applicant's Response filed September 20, 2004, including an RCE and Preliminary Amendment, sought to respond to the objections and rejections issued in the Final Office Action of May 18, 2004, and subsequent Advisory Action of September 1, 2004. For example, Applicant further amended FIG. 5 in response to those Actions, and included comments which resulted in the withdrawal of at least some of the objections and rejections in those Actions. Thus, and based on the comments above, Applicant respectfully submits that the present rejections could not properly have been made in Applicant's earlier application(s) and, therefore, in the event that the application is not passed to allowance, Applicant requests that the finality of the present Office Action be withdrawn.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: February 17, 2005

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